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CLAIMS 1 – 36 (CANCELLED)

Claim 37 (new): A memory device, comprising:

a memory array;

a control circuit, coupled to said memory array;

a input/output circuit, coupled to said memory array; and

a power circuit for supplying an output current to at least one of said memory array, said control circuit, and said input/output circuit, said power circuit comprising:

a first circuit comprising a first input node, a first output node, and a first current mirror;

a second circuit comprising a second input node, a second output node, and a second current mirror;

a third circuit, coupled to said first output node and said second output node, for producing said output current from an input current, said output current being approximately invariant over a range of temperature;

wherein said first current mirror flows a first current as a first function of temperature and said second current mirror flows a second current as a second function of temperature, and said first and second functions are approximately inverse functions of temperature.

Claim 38 (new): The memory device of claim 37, wherein a first output voltage at said first output node is a function of said first current and a second output voltage at said second output node is a function of said second current.

Claim 39 (new): The memory device of claim 38, wherein said third circuit comprises a summing circuit coupled to an output of a first amplifier and an output of a second amplifier, and a gain of said first amplifier is controlled by said first output voltage and a gain of said second amplifier is controlled by said second output voltage.

Claim 40 (new): The memory device of claim 39, wherein said first amplifier is a first transistor and said second amplifier is a second transistor.

Claim 41 (new): The memory device of claim 37, wherein said first current mirror comprises a pair of first control devices and said second current mirror comprises a pair of second control devices.

Claim 42 (new): The memory device of claim 41, said first pair of control devices is a pair of field effect transistors and said second pair of control devices is a pair of bipolar transistors.

Claim 43 (new): A method for supplying power to a memory, comprising:

producing a first control voltage in a first circuit including a first current mirror;

producing a second control voltage in a second circuit including a second current mirror;

amplifying an input current, at a gain controlled by said first control voltage, to produce a first output current;

amplifying the input current, at a gain controlled by said second control voltage, to produce a second output current; and

summing said first output current and said second output current to produce a third output current;

wherein said third output current is approximately invariant over a range of temperatures and said first and second control voltages are approximately inverse functions over said range of temperatures.

Claim 44 (new): The method of claim 43, wherein said first control voltage is produced by dividing a first voltage associated with a first current flowing through a first load coupled to said first current mirror, and said second control voltage is produced by dividing a second voltage associated with a second current flowing through a second load coupled to said second current mirror.

Claim 45 (new): The method of claim 44, further comprising:

controlling said first current via a pair of field effect transistors; and

controlling said second current via a pair of bipolar transistors.

Claim 46 (new): A power circuit, comprising:

a first circuit comprising a first input node, a first output node, and a first current mirror;

a second circuit comprising a second input node, a second output node, and a second current mirror;

a third circuit, coupled to said first output node and said second output node, for producing from an input current, an output current, said output current being approximately invariant over a range of temperature;

wherein said first current mirror flows a first current as a first function of temperature and said second current mirror flows a second current as a second function of temperature, and said first and second functions are approximately inverse functions of temperature.

Claim 47 (new): The power circuit of claim 46, wherein a first output voltage at said first output node is a function of said first current and a second output voltage at said second output node is a function of said second current.

Claim 48 (new): The power circuit of claim 47, wherein said third circuit comprises a summing circuit coupled to an output of a first amplifier and an output of a second amplifier, and a gain of said first amplifier is controlled by said first output voltage and a gain of said second amplifier is controlled by said second output voltage.

Claim 49 (new): The power circuit of claim 48, wherein said first amplifier is a first transistor and said second amplifier is a second transistor.

Claim 50 (new): The power circuit of claim 46, wherein said first current mirror comprises a pair of first control devices and said second current mirror comprises a pair of second control devices.

Claim 51 (new): The power circuit of claim 50, said first pair of control devices is a pair of field effect transistors and said second pair of control devices is a pair of bipolar transistors.

Claim 52 (new): A memory device, comprising:

a memory subsystem; and

a power subsystem, coupled to said memory subsystem and supplying an output current to said memory subsystem, said power subsystem further comprising:

a first current mirror, for supplying at first current to a first load circuit, said first load circuit comprising a field effect transistor and coupled in series with said first current mirror;

a second current mirror, for supplying a second current to a second load circuit, said second load circuit comprising a bipolar transistor and coupled in series with said second current mirror;

a summing circuit, for producing said output current as a sum of a first sub-current and a second sub-current;

wherein

a level of said first sub-current is related to a voltage level of a first control node coupled between said first current mirror and said first load circuit, and

a level of said second sub-current is related to a voltage level of a second control node coupled between said second current mirror and said second load circuit.

Claim 53 (new): The memory device of claim 52, wherein said first load circuit comprises a first field effect transistor and a second field effect transistor, said first and second field effect transistors being coupled, in parallel, to said first current mirror respectively via a first source/drain of said first field effect transistor and a first source/drain of said second field effect transistor.

Claim 54 (new): The memory device of claim 53, wherein a second source/drain of said first field effect transistor is coupled to a resistor.

Claim 55 (new): The memory device of claim 53, wherein a gate of said first field effect transistor is coupled to said first current mirror and a gate of said second field effect transistor is coupled to said first current mirror.

Claim 56 (new): The memory device of claim 52, wherein said second load circuit comprises a first bipolar transistor and a second bipolar transistor, said first and second bipolar transistors being coupled, in parallel, to said second current mirror respectively

via a collector of said first bipolar transistor and a collector of said second bipolar transistor.

Claim 57 (new): The memory device of claim 56, wherein an emitter of said first bipolar transistor is coupled to a resistor.

Claim 58 (new): The memory device of claim 56, wherein a base of said first bipolar transistor is coupled to said second current mirror and a base of said second bipolar transistor is coupled to a base of said second current mirror.

Claim 59 (new): A method for supplying a power signal to a memory circuit in a memory device, said method comprising the steps of:

providing, from a first current mirror, a first current to a first load circuit;

providing a second current to a second load circuit; and

summing a first sub-current and a second sub-current to produce said power signal;

wherein

a level of said first sub-current is related to a first voltage taken between said first current mirror and said first load circuit, and

a level of said second sub-current is related to a second voltage taken between said second current mirror and said second load circuit.

Claim 60 (new): The method of claim 59, wherein said first voltage is supplied as a control voltage to a first amplifier of a first input current and said second voltage is supplied as a control voltage to a second amplifier of said second input current.

Claim 61 (new): The method of claim 60, wherein said first input current is supplied from a same source as said second input current.